III-V 4D Transistors

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J. J. Gu [1)], X. W. Wang [2)], J. Shao [3)], A. T. Neal [1)], M. J. Manfra [3)], R. G. Gordon [2)], and P. D. Ye [1)*]

[1)] *School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906, U.S.A.*

[2)] *Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA 02138, U.S.A.*

[3)] *Department of Physics, Purdue University, West Lafayette, IN, 47906, U.S.A.*

* Tel: 1-765-494-7611, Fax: 1-765-496-6443, Email: yep@purdue.edu

Recently, III-V gate-all-around (GAA) nanowire MOSFETs or III-V 3D transistors have been experimentally demonstrated by a top-down approach [1-2], showing excellent scalability down to channel length (L_{ch}) of 50nm. Although parallel integration of the InGaAs nanowires have been successfully demonstrated in Ref. [1] delivering high drive current per wire, the overall current drivability of the devices are still limited by the relatively large pitch of the nanowires. This limitation would become even more severe with further down-scaling of the nanowire width (W_{NW}) and height (H_{NW}). One elegant solution to improve current drivability is through vertical stacking of nanowires, which has been demonstrated on Si platform [3]. In this work, we have developed a top-down fabrication process to create vertical (normal to the wafer) and lateral (parallel to the wafer) InGaAs nanowire arrays. We call this new type of nanowire devices *III-V 4D transistors* to distinguish them from III-V 3D transistors [1-2] which has only one vertical layer and multiple lateral wires. Furthermore, InGaAs GAA nanowire MOSFETs with 3×4 nanowire array has also been demonstrated for the first time.

Fabrication started with a 2 inch semi-insulating InP (100) substrate. As shown in Fig. 1(a), the following layers were grown sequentially on the InP substrate: a 100nm undoped InAlAs etch stop layer, an 80nm undoped InP sacrificial layer, and then three layers of 30nm $In_{0.53}Ga_{0.47}As$ channel with a 40nm InP layer in between each channel layer. Source/drain implantation was carried out with two-step Si implantation at 20keV and 60keV with a dose of 1×10^{14} cm^{-2}. Fin etching using a novel Cl_2/O_2 chemistry was performed with pre-patterned ALD Al_2O_3 as etch mask. The oxide mask offers much higher selectivity to InGaAs/InP and therefore allows the fabrication of taller fins with H_{fin}=150nm. After fin etching, the sample was soaked in HCl:H_2O (1:2) solution for nanowire release. The HCl based solution selectively removes the InP sacrificial layers underneath each of the InGaAs channel layers provided that the fins were patterned along (100) directions [1]. 10nm Al_2O_3 and 40nm WN was then grown by ALD after surface passivation. WN is a kind of conductive nitride with a high thermal stability and a high work function of ~4.6eV [4]. The ALD process offers smooth (rms roughness 0.2 ~ 0.3 nm), conformal (excellent conformality on a hole sample with 210:1 aspect ratio) and pure WN films with reasonably low conductivity (several mΩ·cm). Cr/Au gate was then defined through a liftoff process and used as the etch mask for the subsequent CF_4/Ar based WN gate etch process. Finally, Au/Ge/Ni based ohmic contacts were formed by e-beam evaporation and liftoff process and the definition of testing pads concludes the fabrication process. All patterns were defined using a UHR Vistec VB6 e-beam lithography system. Fig. 1 shows the schematic diagram of the device structure as an orthographic projection and a cross-sectional view of the vertically stacked nanowires. Fig. 2 summarized key fabrication process steps.

Fig. 3 (a) shows the top view SEM image of a finished device, showing parallel integration of 4 nanowire stacks laterally on the wafer. Fig. 3 (b) shows the cross sectional TEM image of one of these stacks, showing the 3 vertical stacked nanowires. The Al_2O_3 dielectric and WN gate metal was clearly observed around all the wires, confirming the conformality of the ALD process. Due to the non-vertical fin etching process, the W_{NW} increases from ~20nm for layer 1, ~60nm for layer 2, to ~100nm for layer 3, with a fixed H_{NW} of 30nm for all three layers defined by the MBE growth thickness. More vertical dry etching process is under development. However, the stacked nanowires with different size could also be beneficial for better linearity than the uniform wires for RF device applications [5]. Fig. 3(c) shows the vertical and lateral integration of a 3×4 InGaAs nanowire array. Fig. 4 shows the output characteristics of a typical device with 3×4 nanowire array with L_{ch}=200nm. The maximum saturation current reaches ~3mA at V_{ds}=1V and V_{gs}=2V. Normalization by total perimeter of the 12 nanowires yields a high drive current of 1.35mA/μm. If normalized only by the average dimension (60nm), I_{ds}≈12mA/ μm. As shown in Fig. 5, peak transconductance of 0.6mS/μm and 0.85mS/μm (5.4mS/μm and 7.7mS/μm normalized by the average dimension) was obtained at V_{ds} of 0.5V and 1V, respectively.

In conclusion, we fabricated for the first time vertically and laterally integrated III-V 4D transistors. III-V GAA nanowire MOSFETs with 3×4 arrays show high drive current of 1.35mA/μm and high transconductance of 0.85mS/μm. The vertical stacking of the III-V nanowires have provided an elegant solution to the drivability bottleneck of nanowire devices and is promising for future low-power logic and RF application.

References: [1] J. J. Gu et al., IEDM Tech. Dig. 769, 2011. [2] J. J. Gu, et al., IEEE Electron Device Lett. in press. [3] W. W. Fang et al., IEEE Electron Device Lett. **28**, p. 211, 2007. [4] J. S. Becker et al., Chem. Mat., **15**, 2969 2003. [5] X. L. Li et al., private communications.

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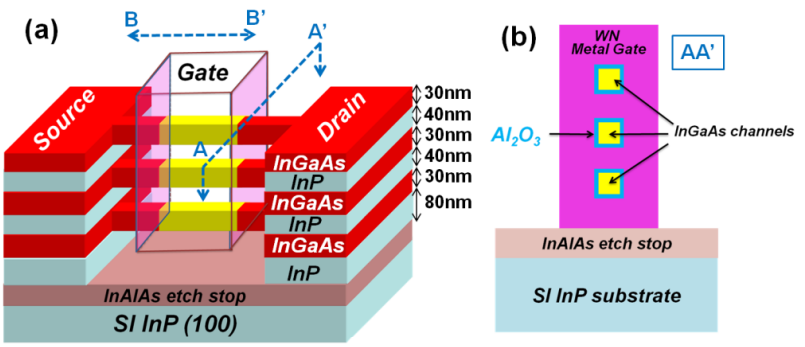

Fig. 1 (a) Schematic diagram of vertically stacked (3×1) InGaAs GAA nanowire MOSFETs. **(b)** Cross sectional view of the 3-layer vertically stacked InGaAs nanowires along AA'.

Fig. 2 Fabrication process flow for vertically stacked InGaAs GAA nanowire MOSFETs.

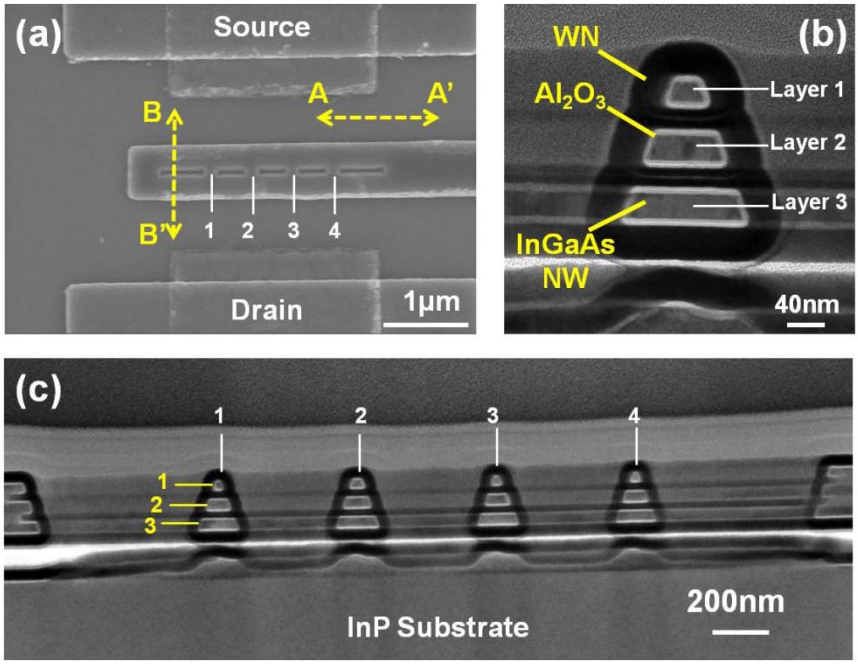

Fig. 3 (a) Top-view SEM image of a vertically stacked InGaAs GAA nanowire MOSFETs with 4 parallel nanowire stacks. AA' and BB' correspond to the direction in Fig. 1(a).

(b) Cross sectional high resolution TEM image of a InGaAs nanowire stack. The nanowires are wrapped by 10nm ALD Al_2O_3 gate dielectric and 40nm ALD WN metal gate. The W_{NW} increase from layer 1 through layer 3 due to the non-vertical fin dry etching process. The W_{NW} for layer 1, 2 and 3 are measured to be around 20, 60, and 100nm. The H_{NW} for each layer is 30nm. Therefore the total perimeter of a 3×1array is ~540nm.

(c) The cross sectional TEM image of the 3×4 nanowire array along A-A'.

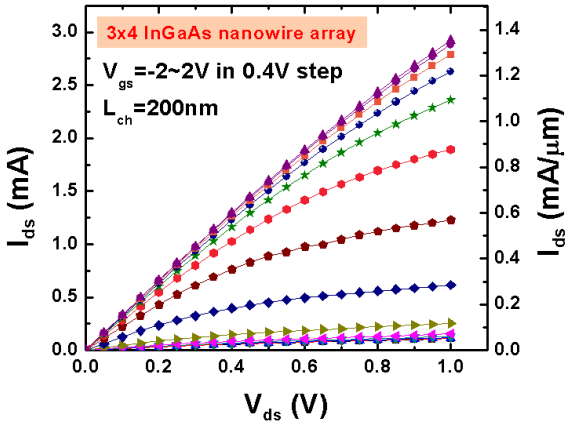

Fig. 4 Output characteristics of vertically stacked InGaAs GAA nanowire MOSFETs with 3×4 nanowire array. The maximum saturation current reaches 1.35mA/μm at V_{ds}=1V and V_{gs}=2V normalized by total perimeter of the nanowires.

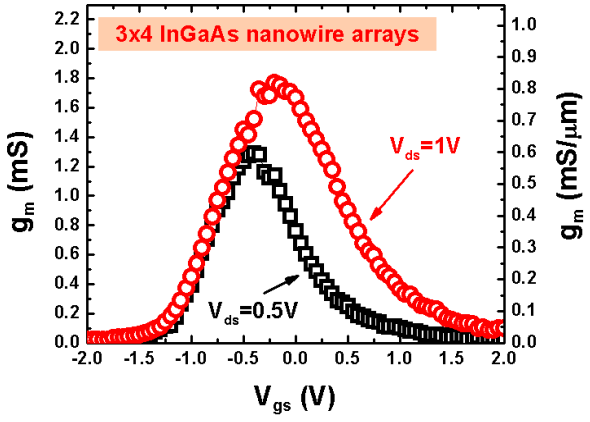

Fig. 5 g_m-V_{gs} of vertically stacked InGaAs GAA nanowire MOSFETs with 3×4 nanowire array. The maximum g_m reaches 0.85mS/μm at V_{ds}=1V and 0.6mS/μm at V_{ds}=0.5V normalized by total perimeter of the nanowires.